Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**GATE**

**SOURCE**

**.148”**

**.106”**

**Top Material: Al**

**Backside Material: CrNiAg**

**G = .018” X .025”**

**S = .029” X .041”**

**Backside Potential: Drain**

**Mask Ref: Gen 3**

**APPROVED BY: DK DIE SIZE .106” X .148” DATE: 7/11/22**

**MFG: INT’L RECTIFIER THICKNESS .014” P/N: IRFC130**

**DG 10.1.2**

#### Rev B, 7/19/02